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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,726	MARISETTY ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-23* is/are allowed.

6)☒ Claim(s) *1-19 and 24-26* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 24-26 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 24 claims a recording medium on which a program is stored and variations thereof. These claims therefore are interpreted as recording a program per se. In order to overcome this rejection, language, specifically stating the claim, **must be** limited to a computer program stored on a computer recordable medium executing on a computer.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-16 and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Bowers, U.S. Patent 6,308,285 B1.

Referring to claim 1:

a. In column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (non-volatile memory in which is stored an error handling routine). Further, in column 4, lines 57-59, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode (an error handling routine).

b. In column 2, lines 60-62, Bowers discloses that after the failed processor is replaced all the processors are awakened and the computer is returned to normal operation without the need to reboot the computer (said error handling routine to permit a computer system to continue operating when an error is detected).

c. In Figure 1, Bowers discloses a plurality of processors included in the computer system connected to a shared memory. In column 3, lines 45-59, Bowers discloses that the non-volatile memory stores an operating system.

d. In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. To achieve this, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS (each processor is capable of accessing the error handling routine). This routine stores information in non-volatile RAM. Further, the sleep signals are delivered to each processor via the respective buses

(detecting an error and signaling the remaining processors of the plurality of processors to enter a rendezvous state).

Referring to claim 2, in column 2, lines 49-62, Bowers discloses replacing one or more of the processors by placing all the processors in a sleep mode (wherein the error is only correctable entering the rendezvous state).

Referring to claim 3, in column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs (a processor abstraction layer located in the non volatile memory, wherein the processor abstraction layer includes the error handling routine).

Referring to claims 4 and 6, in column 4, lines 57-65, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS (a system abstraction layer located in the non volatile memory wherein the system abstraction layer includes the error handling routine).

Referring to claim 5:

a. In column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software

programming, memory is coupled to the processors to store and to facilitate execution of these programs (non-volatile memory to store an error handling routine and an idle routine). Further, in column 4, lines 57-59, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode (an error handling routine and idle routine).

b. In column 2, lines 60-62, Bowers discloses that after the failed processor is replaced all the processors are awakened and the computer is returned to normal operation without the need to reboot the computer (said error handling routine to permit a computer system to continue operating when an error is detected).

c. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs (a plurality of slave processors to execute the idle routine). Further, in Figure 1, Bowers discloses that the plurality of slave processors are included in the computer system.

d. In column 5, lines 2-3, Bowers discloses a controller (monarch processor included in the computer system) that generates a stop clock signal STPCLK# and a sleep signal SLP# (error handling routine to correct an error).

Referring to claim 7, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (wherein the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state).

Referring to claim 8:

a. In Figure 2, Bowers discloses a multiprocessor computer system (a plurality of processors) and a PAL controller (a monarch processor).

b. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs. An interface between the signals generated by the controller and the processors so that there is a processor abstraction layer coupled to the plurality of processors is inherent to the system.

c. In column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS. The routine generates a "start" signal and delivers it to the

controller via the bridge/memory controller. An interface between the _PTS routine and the controller so that there is a system abstraction layer coupled to the processor abstraction layer is inherent to the system.

d. In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer to initiate a rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (ending the rendezvous state).

e. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (said rendezvous state being a state where all but one of said processors in said plurality of processors are idle).

Referring to claim 9, in column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (the processor abstraction layer is located in the non volatile memory and is executed by the plurality of processors, and the system abstraction layer is located in the non volatile memory and is executed by the plurality of processors). Further, in column 4, lines 40-42, Bowers discloses an operating system of the

computer (the operating system layer is located in the system memory and executed by the plurality of processors).

Referring to claim 10, in column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS (error handling routine included in the system abstraction layer). The routine generates a "start" signal and delivers it to the controller (monarch processor) via the bridge/memory controller. Further, in column 5, lines 10-13, Bowers discloses that after the processors have been placed into the sleep state (rendezvous state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal (the monarch processor executing an error handling routine included in the system abstraction layer upon initiation of the rendezvous state).

Referring to claim 11, in column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs (the processor abstraction layer includes a functional module for error handling).

Referring to claim 12:

a. In Figure 2, Bowers discloses a multiprocessor computer system (a plurality of processors).

b. In column 3, lines 45-48, Bowers discloses that because the processors control the functioning of the system generally under the control of software programming, memory is coupled to the processors to store and to facilitate execution of these programs (a processor abstraction layer is located in a non volatile memory coupled to the plurality of processors, and a system abstraction layer located in the non volatile memory).

c. Further, in column 4, lines 40-42, Bowers discloses an operating system of the computer (an operating system layer located in a system memory coupled to the plurality of processors).

d. In column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit. The processors also stop executing commands and tri-state some outputs. An interface between the signals generated by the controller and the processors so that there is a processor abstraction layer coupled to the plurality of processors is inherent to the system.

e. In column 4, lines 57-67 continued in column 5, line 1, Bowers discloses that an ACPI-compliant operating system interprets the SCI interrupt and

prepares to place the identified processor into a sleep mode. Specifically, the processor will be placed into an ACPI "S2" sleep state. To achieve this result, the operating system services the SCI interrupt by calling a _PTS routine stored in the ROM/BIOS. The routine generates a "start" signal and delivers it to the controller via the bridge/memory controller. An interface between the _PTS routine and the controller so that there is a system abstraction layer coupled to the processor abstraction layer is inherent to the system.

f. In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (an interrupt signaling mechanism coupled to the processor abstraction layer, the system abstraction layer, and the operating system layer for initiation of a rendezvous state to initiate a rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (ending the rendezvous state upon receiving a signal that error handling is completed).

g. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (said rendezvous state being a state where all but one of said processors in said plurality of processors are idle).

Referring to claim 13, in column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the

processors (wherein the signal from the operating system to end the rendezvous state is an interrupt).

Referring to claim 14, In column 4, lines 57-67 continued in column 5, lines 1-9, Bowers discloses a sleep state signal that is passed from the operating system to the processors (the processor abstraction layer is capable of sending a signal to the system abstraction layer to enter the rendezvous state). Further, in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (performing error handling upon entering the rendezvous state).

Referring to claim 15:

a. In column 7, lines 1-4, Bowers discloses that if multiple processors are to be removed or replaced these processors may be identified by a failure detection system or by the user via a software or hardware interface (detecting an error by one processor included in a multiple processor system).

b. In column 5, lines 2-13, Bowers discloses placing the processors in a sleep state (entering a rendezvous state in which all processors but the one processor included in the multiple processor system are idle).

c. In column 5, lines 10-13, Bowers discloses that after the processors have been placed into the sleep state (rendezvous state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal (correcting the error using the one processor).

d. In column 2, lines 60-62, Bowers discloses that after replacement of the processor, all processors are awakened and the computer is returned to normal operation without the need to reboot the computer (resuming normal operation).

Referring to claim 16, in column 5, lines 2-13, Bowers discloses placing the processors in a sleep state (requesting a plurality of processors included in the multiple processor system to enter an idle state) and that after the processors have been placed into the sleep state (waiting until the plurality of processors have entered the idle state), the controller delivers a reset signal RESET# to the processor being removed, followed by de-assertion of the PWRGOOD signal.

Referring to claim 24:

a. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (attempting to correct an error by a detecting processor included in a multiple processor system).

b. In column 4, lines 60-62, Bowers discloses that the operating system services the SCI interrupt (error) by calling a _PTS routine stored in the ROM/BIOS (on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error).

c. In column 5, lines 2-9, Bowers discloses placing the processors in a sleep state and having a controller not in the sleep state (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of said processors included in the multiple processor system are idle).

Referring to claim 25, in column 5, lines 2-9, Bowers discloses placing the processors in a sleep state (wherein all but the one of the processors included in the multiple processor system are executing a spin loop) and having a controller not in the sleep state.

Referring to claim 26, in column 5, lines 2-9, Bowers discloses that a controller generates a stop clock signal STPCLK# and a sleep signal SLP#. These signals are delivered to each processor via a respective bus. These signals place the processors into a low power state so that they stop providing internal clock signals to all units except the bus unit and the APIC unit (informing a processor abstraction layer when all but one of the processors included in the multiple processor system have entered the idle state).

5. Claims 18 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Falik et al., U.S. Patent 6,065,078.

Referring to claim 18:

a. In column 1, lines 34-48, Falik et al. disclose that the debugger interface sends a debugger command to at least one of the plurality of processors (attempting to correct an error by a detecting processor included in a multiple processor system).

b. In column 4, lines 41-47, Falik et al. disclose sending an interrupt to a processor, which stops the execution of the application program and starts to execute the monitor (on failure, executing firmware code operatively coupled to all the processors included in the multiple processor system to correct the error).

c. In column 7, lines 26-30, Falik et al. disclose that the interrupt control module issues an ISE interrupt request to either a specific one of the processors or to multiple processors (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle).

Referring to claim 19:

a. The debugger interface of Falik et al. is pre-designated making it the monarch processor from the processors included in the multiple processor system.

b. In column 4, lines 41-47, Falik et al. disclose sending an interrupt to a processor, which stops the execution of the application program (signaling slave processors included in the multiple processor system to execute a spin loop) and starts to execute the monitor (correcting the error by the monarch processor).

d. In column 2, lines 43-46, Falik et al. disclose that after the phase of debugging software for the processors of the multiprocessor integrated circuit, the multiprocessor integrated circuit would, in most cases, no longer interact with the host computer (resuming normal operation by the plurality of processors).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bowers, U.S. Patent 6,308,285 B1, and further in view of Fujii et al., U.S. Patent 5,892,898. In column 2, lines 49-62, Bowers discloses removing or replacing one or more of the processors for various reasons. However, Bowers doesn't explicitly disclose determining if the error is a severe error and only upon determining that the error is a severe error, entering the rendezvous state. In column 2, lines 14-19, Fujii et al. disclose an event message that corresponds to an event type that includes at least one event type selected from the group consisting of an information event type, a warning event type, and an error event type. It would have been obvious to one of ordinary skill at the time of the invention to include the event categorizing method of Fujii et al. into the system of Bowers. A person of ordinary skill in the art would have been motivated to make the modification because an error event type is used to report a non-recoverable problem (see Fujii et al.: col.2, lines 62-63) and a warning event type is used to indicate some kind of recoverable anomaly (see Fujii et al.: col. 2, lines 60-62). Knowing the severity determines what action should be taken (removal of a processor) (see Fujii et al.: col. 2, lines 48-55).

Allowable Subject Matter

8. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 21-23 are allowed.

10. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or reasonably suggest executing a spin loop routine in a second firmware layer by the plurality of processors except the monarch processor and accessing a routine in the second firmware layer to correct the error.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT W BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100